Cross-Platform FPGA Accelerator Development Using CoRAM and CONNECT

Eric S. Chung
Microsoft Research Silicon Valley
Mountain View, CA
erchung@microsoft.com

Michael K. Papamichael, Gabriel Weisz,
James C. Hoe
Carnegie Mellon University
Pittsburgh, PA
{papamix, gweisz}@cs.cmu.edu,
jhoe@ece.cmu.edu

ABSTRACT
The CoRAM memory architecture is an easy-to-use and portable abstraction for FPGA accelerator development [1, 2]. Using the CoRAM framework, FPGA developers can write their applications once and re-target them automatically to different FPGA platforms and devices (e.g., Xilinx ML605, Altera DE4, ZYNQ-702, etc). In this tutorial, participants will learn the key concepts of the CoRAM Virtual Architecture and the underlying CONNECT Network-on-Chip generation framework [3]. The tutorial is organized into three parts. The first part will provide an overview of the CoRAM Virtual Architecture and include a hands-on section where participants will work on a small example to get first-hand experience with the CoRAM development flow. The second part of the tutorial will provide a beneath-the-hood look at CoRAM and cover more advanced topics. These topics include memory loading, user I/O, debugging, as well as a segment on the CONNECT NoC generation framework which serves as the on-chip interconnect for CoRAM. The final part of the tutorial will be devoted to more advanced exercises and demos, as well as a Q&A session for CoRAM and CONNECT. The tutorial assumes a basic understanding of RTL design and C programming. To join in on the hands-on exercise, the attendees need laptops with 15GB of free space and VirtualBox installed. Please visit http://www.ece.cmu.edu/~coram for information about CoRAM and updates on this tutorial.

Categories and Subject Descriptors
C.0 [Computer System Organization]: System Architectures

Keywords
FPGA computing, memory architecture, Network-on-Chip

REFERENCES

Copyright is held by the author/owner(s). 
FPGA ’13, February 11–13, 2013, Monterey, California, USA. 
ACM 978-1-4503-1887-7/13/02.