Wednesday, February 13

All day  Registration
Steinbeck Lobby, Monterey Conference Center

8:00 AM  Continental Breakfast
Ferrantes, Monterey Conference Center

9:00 AM  Session 5: FPGA Architecture
Session Chair: Peter Cheung, Imperial College
Steinbeck Forum, Monterey Conference Center

Location, Location, Location---The Role of Spatial Locality in Asymptotic Energy Minimization
Andre DeHon

Architectural Enhancements in Stratix V
David Lewis, David Cashman, Mark Chan, Jeff Chromczak, Gary Lai, Andy Lee, Tim Vanderhoek and Haiming Yu

Minimum Energy Operation for Clustered Island-Style FPGAs
Peter Grossmann, Miriam Leeser and Marvin Onabajo

Improving Bitstream Compression by Modifying FPGA Architecture (Short)
Seyyed Ahmad Razavi and Morteza Saheb Zamani

10:05 AM  Poster Session III (55 minutes)
Colton Room, Monterey Conference Center

Effect of Fixed-Point Arithmetic on Deep Belief Networks
Jingfei Jiang, Rongdong Hu and Mikel Lujan

A Memory-efficient Hardware Architecture for Real-time Feature Detection of the SIFT Algorithm
Wenjuan Deng and Yiqun Zhu

Exploiting Algorithmic-Level Memory Parallelism in Distributed Logic-Memory Architecture through Hardware-Assisted Dynamic Graph
Mingjie Lin

FPGA-Based HPC Application Design for Non-Experts
David Uliana, Krzysztof Kepa and Peter Athanas

AutoMapper - An Automated Tool for Optimal Hardware Resource Allocation for Networking Applications on FPGA
Swapnil Haria and Viktor Prasanna

Performance and Toolchain of a Combined GPU/FPGA Desktop
Bruno da Silva, An Braeken, Erik H. D'Hollander, Abdellah Touhafi, Jan G. Cornelis and Jan Lemeire
Hardware Description and Synthesis of Control-Intensive Reconfigurable Dataflow Architectures
Marc-Andre Daigneault and Jean Pierre David

Automating Resource Optimisation in Reconfigurable Design
Xinyu Niu, Thomas C.P. Chau, Qiwei Jin, Wayne Luk and Qiang Liu

11:00 AM  **Session 6: Design Studies and Design Methodologies**
Session Chair: James Hoe, Carnegie-Mellon University
Steinbeck Forum, Monterey Conference Center

*Elastic CGRAs*
Yuanjie Huang, Olivier Temam, Paolo Ienne, Yunji Chen and Chengyong Wu

*Embedding-Based Placement of Processing Element Networks on FPGAs for Physical Model Simulation*
Bailey Miller, Frank Vahid and Tony Givargis

*Area-Efficient Near-Associative Memories on FPGAs*
Udit Dhawan and Andre DeHon

12:00 PM  **Lunch (1 hour 45 minutes)**
Ferrantes, 10th Floor, Marriott Hotel