1:45 PM  **Session 7: High-Level Abstractions and Tools**  
**Session Chair:** Mike Hutton, Altera  
*Steinbeck Forum, Monterey Conference Center*

**Dynafuse: Dynamic Dependence Analysis for FPGA Pipeline Fusion and Locality Optimizations**  
Jeremy Fowers and Greg Stitt

**A Remote Memory Access infrastructure for Global Address Space programming models in FPGAs**  
Ruediger Willenberg and Paul Chow

**C-To-CoRAM: Compiling Perfect Loop Nests to the Portable CoRAM Abstraction**  
Gabriel Weisz and James Hoe

**Architecture support for custom instructions with memory operations (short)**  
Jason Cong and Karthik Gururaj

2:50 PM  **Poster Session IV (55 Minutes)**  
*Colton Room, Monterey Conference Center*

**Low Power FPGA Design Using Post-silicon Device Aging**  
Sheng Wei, Jason Zheng and Miodrag Potkonjak

**Circuit Optimizations to Minimize Energy in the Global Interconnect of a Low-Power FPGA**  
Oluseyi Ayorinde and Benton Calhoun

**Efficient System-Level Mapping from Streaming Applications to FPGAs**  
Jason Cong, Muhuan Huang and Peng Zhang

**Defect Recovery in Nanodevice-Based Programmable Interconnects**  
Jason Cong and Bingjun Xiao

**A High-Performance, Low-Energy FPGA Accelerator for Correntropy-Based Feature Tracking**  
Patrick Cooke, Jeremy Fowers, Lee Hunt and Greg Stitt

**Scalable High-throughput Architecture for Large Balanced Tree Structures on FPGA**  
Yun Qu and Viktor Prasanna

**Co-simulation framework of SystemC SoC Virtual Prototype and Custom Logic**  
Nick Ni and Yi Peng

**Rectification of Advanced Microprocessors without Changing Routing on FPGAs**  
Satoshi Jo, Amir Masoud Gharehbaghi, Takeshi Matsumoto and Masahiro Fujita
Shadow AICs: Reaping the Benefits of And-Inverter Cones with Minimal Architectural Impact  
Hadi Parandeh Afshar, David Novo Bruna, Grace Zgheib, Madhura Purnaprajna and Paolo Ienne

3:45 PM  
**Session 8: Applications II**  
Session Chair: Steve Trimberger, Xilinx  
Steinbeck Forum, Monterey Conference Center

**An FPGA Based Parallel Architecture For Music Melody Matching**  
Hao Wang and Jyh-Charn Liu

**An FPGA Memcached Appliance**  
Sai Rahul Chalamalasetti, Kevin Lim, Mitch Wright, Parthasarathy Ranganathan, Alvin Auyoung and Martin Margala

**High Throughput and Programmable Online Traffic Classifier on FPGA**  
Da Tong, Lu Sun, Kiran Matam and Viktor Prasanna

4:45 PM  
**Best Paper Award and Closing Remarks**  
Vaughn Betz and Brad Hutchings  
Steinbeck Forum, Monterey Conference Center