ABSTRACT
Engineering complex systems inevitably requires a designer to balance many conflicting design requirements including performance, cost, power, and design time. In many cases, FPGAs enable engineers to balance these design requirements in ways not possible with other technologies like ASICs, ASSPs, GPUs or general purpose processors. This tutorial will focus on two of the newest commercial FPGA-related technologies, High Level Synthesis (HLS) and Programmable Logic integrated tightly with high performance embedded processors. In particular, we will present a detailed introduction to Vivado® HLS, which is capable of synthesizing optimized FPGA circuits from algorithmic descriptions in C, C++ and SystemC. We will also present an introduction to the architecture of Zynq® devices and show how interesting system architectures can be constructed using High Level Synthesis and the programmable logic portion of these devices.

The tutorial will focus on the practical application of HLS and Zynq® to build real systems. It will demonstrate both HLS and system-level optimization techniques and ways to identify and eliminate bottlenecks in computation and communication. In addition, the tutorial will draw from a number of application areas including video, wireless communications, and medical imaging.

Vivado® HLS can be downloaded as a part of the Vivado® Design Suite. Evaluation licenses are available with a xilinx.com website account. Academic licenses can be requested through the Xilinx® University Program. Multiple Zynq® boards are available, including the ZC702, ZC706, and the community zedboard.

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